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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,540	08/28/2000	Alexander D. Schapira	246/214	7789

23639 7590 08/11/2005

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EXAMINER
ORTIZ RODRIGUEZ, CARLOS R

ART UNIT	PAPER NUMBER
2125	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/648,540	SCHAPIRA ET AL.	
	Examiner	Art Unit	
	Carlos Ortiz-Rodriguez	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/23/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-7 and 9-18* is/are allowed.

6)☒ Claim(s) *1,2 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 05/23/2005 have been fully considered. Applicant's arguments with respect to claims 1, 2 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

2. Claims 3-7 and 9-18 are allowed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1, 2, and 8 rejected under 35 U.S.C. 102(e) as being anticipated by Nair et al. U.S Patent No. 6,090,149.

Regarding claims 1, 2, and 8 Nair et al. discloses a circuit design simulator, comprising:
a stored electronic representation of a circuit design (C6 L1-20),
said circuit design including at least one interface between a digital circuit and an analog circuit,
said interface comprising a node at which said digital circuit provides an output and at which said analog circuit receives an input and provides a conditional output (C4 L40-65),
said output taking on any one of several states including a digital high state, digital low state, or a high impedance state (C2 L32-38). Furthermore Nair et al. discloses at least one processor for simulating operation of said circuit design, said at least one processor dynamically determining whether or not to apply each conditional output to its respective node according to the state of the digital circuit output connected to the node (C3 L20-30).

Citation of Pertinent Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to method and system for simulation of digital/analog interfaces with analog tri-state ioputs:

a. U.S. Pat. No. 6,100,830 to Dedic, which discloses differential switching circuitry.

The following publications are cited to further show the state of the art with respect to method and system for simulation of digital/analog interfaces with analog tri-state ioputs:

b. Thelen et al., "Simulating Mixed Analog-Digital Circuits on a Digital Simulator", IEEE, 1988.

c. IEE Proceedings, Vol. 136, PT. G, No. 3, June 1989.

d. Shi et al., "Use of VHDL to Model and Simulate Analog-Digital IC's", IEEE, 1992.

e. Minoura et al., "Structural Active Object Systems for Simulation", ACM, 1993.

f. Chamberlain, "Parallel Logic Simulation of VLSI Systems", ACM, 1995.

g. Low et al., "Cadence-based simulation of floating-gate circuits using the EKV model", IEEE, 1999.

h. Yuan et al., "Floating-point analog-to-digital converter", IEEE, 1999.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carlos Ortiz-Rodriguez whose telephone number is (571) 272-3747. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on (571) 272-3749. The central official fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the general information number at 800-786-9199.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Carlos Ortiz-Rodriguez
Patent Examiner
Art Unit 2125

cror

August 7, 2005

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100